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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,879	09/14/2006	Yoshiyuki Murakami	Q96906	1714

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EXAMINER	
VO, NGUYEN THANH	

ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,879	MURAKAMI ET AL.	
	Examiner	Art Unit	
	NGUYEN VO	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 7-8, 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 2003/0189910) in view of Toncich (US 2007/0207748).

As to claim 1, Yamada discloses in figure 49 a high-frequency circuit for branching high-frequency signals for pluralities of communications systems of different frequencies, which comprises a lowpass filter circuit disposed between first and second ports (see the LPF) and/or a highpass filter circuit disposed between said first port and a fourth port (see the HPF); and a bandpass filter circuit disposed between said first port and a third port (see the BPF); said lowpass filter circuit, said highpass

filter circuit comprising capacitance elements and inductance elements (see figure 50); said bandpass filter circuit being a SAW filter (see paragraph [0484]); and the passband f1 of said lowpass filter circuit, the passband f2 of said bandpass filter circuit, and the passband f3 of said highpass filter circuit meeting the condition of f1< f2< f3 (in this case, f1=[880-960]; f2=[1710-1980]; f3=[2110-2305] as shown in figure 49; therefore, f1<f2<f3). Yamada fails to disclose a matching circuit as claimed. Toncich discloses in figure 11 an antenna matching circuit 163 comprising capacitance elements and inductance elements (see figure 7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above teaching of Toncich to Yamada, in order to reduce the power loss (as suggested by Toncich at paragraph [0068]).

As to claim 2, the combination of Yamada and Toncich fails to disclose that the inductance element (see figure 7 of Toncich) has a Q value of 20 or more at 250 MHz to absorb electrostatic surge as claimed. Those skilled in the art, however, would have recognized that the above claimed limitation would not render the claim patentable over the combination of Yamada and Toncich, because it would merely depend on how much one would like to set the Q value of his/her matching circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the above combination of Yamada and Toncich such that the inductance element (see figure 7 of Toncich) has a Q value of 20 or more at 250 MHz, in order to reduce electrostatic surge at a desired level.

As to claim 3, the combination of Yamada and Toncich fails to disclose a diplexer as claimed. The examiner, however, takes Official Notice that such a diplexer is known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a conventional diplexer to the above combination of Yamada and Toncich, in order to provide more isolation between different operating frequency bands.

As to claim 4, Yamada further discloses a switch as claimed (see switch 2306, switch 2307 in figure 49).

As to claim 7, Yamada further discloses a multi-band antenna ANT (see figure 49).

As to claim 8, first of all it is rejected for similar reasons as set forth in claim 1 above. In addition, Yamada further discloses in figure 9(a) that the substrate contains the inductors and capacitors, and that the SAW filter and the remaining circuit elements (see "Chip parts" in figure 9(a)) are mounted onto the substrate. The combination of Yamada and Toncich fails to disclose that the substrate in figure 9(a) of Yamada is a laminate substrate as claimed. The examiner, however, takes Official Notice that such a laminate substrate is known in the art (for example, see the present specification, paragraph [0012]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the substrate in figure 9(a) of Yamada with a conventional laminate substrate, because the laminate substrate has advantages such as low cost, efficient heat dissipation, scale reduction.

As to claim 10, see Toncich, figure 11; paragraph [0015].

As to claims 11-12, the combination of Yamada and Toncich fails to disclose that the core of the inductance element in figure 7 of Toncich is made of non-magnetic, alumina-based ceramic material as in claim 11, and ground electrode and LGA terminal electrodes as in claim 12. The examiner, however, takes Official Notice that such claimed limitations are known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the above combination as claimed, in order to reduce the size and cost of the high-frequency device.

As to claim 13, see figure 49 of Yamada; in this case, f1=[880-960]; f2=[1710-1980]; f3=[2110-2305]; therefore, f1<f2<f3.

4. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Toncich as applied to claim 1 above, and further in view of Kearns (US 2004/0132487).

As to claim 5, the combination of Yamada and Toncich fails to disclose that the SAW filter comprising a balanced port connected to said third port, and an unbalanced port connected to said first port as claimed. Kearns discloses a SAW filter (see SAW filters 30, 32, 34 in figure 6a; see also paragraph [0059]) comprising a balanced port connected to a third port (see node 16B), and an unbalanced port connected to a first port (see node C). See Kearns, paragraph [0050]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above teaching of Kearns to the above combination of Yamada and Toncich, because the SAW filters have addition benefit of being capable of providing unbalanced to balanced conversion (as suggested by Kearns at paragraph [0050]).

As to claim 6, as the combination of Yamada and Toncich is modified with the SAW filters of Kearns for the reasons as set forth in claim 5 above, it would further read on the claimed limitation.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Toncich as applied to claim 8 above, and further in view of Harihara (US 7,023,385).

As to claim 9, the combination of Yamada and Toncich fails to disclose that the circuit elements do not overlap each other in a laminate direction of the laminate substrate as claimed. Harihara discloses that that the circuit elements do not overlap each other in a laminate direction of the laminate substrate (see abstract; column 2 lines 20-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above teaching of Harihara to the above combination of Yamada and Toncich, in order to reduce signal interference (as suggested by Harihara at column 2 lines 32-36).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hagn (US 2002/0090974); Satoh (US 2002/0137471); Uriu (US 2003/0092397); Forrester (US 7,376,440) disclose multiband high-frequency devices.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGUYEN VO whose telephone number is (571)272-7901. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nguyen Vo/
Primary Examiner, Art Unit 2618
09/11/2008